



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/880,458	06/12/2001	Roger May	015114-053400US	5231

26059 7590 09/15/2003

TOWNSEND AND TOWNSEND AND CREW LLP/ 015114  
TWO EMBARCADERO CENTER  
8TH FLOOR  
SAN FRANCISCO, CA 94111-3834

EXAMINER

TAN, VIBOL

ART UNIT PAPER NUMBER

2819

DATE MAILED: 09/15/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

09/880,458

Applicant(s)

MAY ET AL.

Examiner

Vibol Tan

Art Unit

2819

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 12 June 2001.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 1-42 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 39,41 and 42 is/are allowed.
- 6) ☒ Claim(s) 1-4,19,20,22,28,38 and 40 is/are rejected.
- 7) ☒ Claim(s) 5-14,16-18,21,23-27,29-32 and 34-37 is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some \* c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- \* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 5,6.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: \_\_\_\_\_.

## **DETAILED ACTION**

### ***Drawings***

1. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the snoop circuitry must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

### ***Claim Objections***

2. Claim 4 is objected to because of the following informalities: in line 6, change "...the output..." to "...an output..." Appropriate correction is required.

### ***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-4, 19, 20, 22, 28, 33, 38, and 40 are rejected under 35 U.S.C. 102(b) as being anticipated by Ashby et al. (U. S. PAT. 5,347,181).

In claim 1, Ashby teaches all claimed features in Figs. 1-11, an integrated circuit, comprising: programmable logic circuitry (16); embedded processor circuitry comprising a processor (12); and shared I/O circuitry (14) coupled to the embedded

processor circuitry (12) and the programmable logic circuitry (16) that comprises a plurality of I/O pins (22, 23, 24; abs.) which are accessible by the processor and the programmable logic circuitry.

In claim 2, Ashby further teaches all claimed features in Figs. 1-11 the integrated circuit of claim 1 wherein the shared I/O circuitry (14) further comprises a plurality of output driver circuits (54, 72), each coupled to one of the I/O pins (56, 74), that drive signals sent to the I/O pins.

In claim 3, Ashby further teaches all claimed features in Figs. 1-11 the integrated circuit of claim 1 wherein the shared I/O circuitry further comprises a plurality of input driver circuits (167, 195), each coupled to one of the I/O pins (166, 191), that drive signals received on the I/O pins.

In claim 4, Ashby further teaches all claimed features in Figs. 1-11, the integrated circuit of claim 1 wherein the shared I/O circuitry (14) further comprises: a first multiplexer (50) coupled to receive a first data signal (SIG\_FROM\_ASIS) from the programmable logic circuitry (16) at a first input (I1) and a second data signal (SIG\_FROM\_UP) from the embedded processor circuitry (12) at a second input (I0); and a driver circuit (54) that drives an output (OUT) of the first multiplexer onto a first one (56) of the I/O pins.

In claim 15, Ashby further teaches all claimed features in Figs. 1-11, the integrated circuit of claim 1 wherein data bits (inherency) are loaded into the programmable logic circuitry through the I/O pins of the shared I/O circuitry to configure the programmable logic circuitry.

Claim 19 is essentially the same in scope as claim 1; therefore, it is rejected in the same manner.

Method claims 20 and 22 are essentially the same in scope as apparatus claims 1 and 4; therefore, they are rejected in the same manner.

Method claim 28 is essentially the same in scope as apparatus claim 1; therefore, it is rejected in the same manner.

In claim 33, Ashby teaches all claimed features in Figs. 1-11, an integrated circuit, comprising: a programmable logic portion (10); an embedded logic portion (16) adjacent to a first edge (bottom edge) of the integrated circuit, the embedded logic portion comprising a processor (12); and a shared I/O portion (14) in between the programmable logic portion and the embedded logic portion, the shared I/O portion comprising first I/O pins (22, 23, 24) that are accessible by circuitry in the programmable logic portion and the embedded logic portion.

Method claim 38 is essentially the same in scope as apparatus claim 33; therefore, it is rejected in the same manner.

Method claim 40 is essentially the same in scope as apparatus claim 33; therefore, it is rejected in the same manner.

5. Claims 5-14, 16-18, 21, 23-27, 29-32, and 34-37 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

6. Claims 39, 41, and 42 appear to comprise allowable subject matters.

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Chang teaches an embedded configurable ASIC. Gilson teaches a fault-tolerant waferscale integrated circuit device and method. Cherichetti et al. teaches test method matrix circuit for an embedded microprocessor core.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (703) 306-5948. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (703) 305-3493. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0959.

Vibol Tan



Patent Examiner, AU 2819